DR11-C
general device
interface manual

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CHAPTER 1
INTRODUCTION

1.1 INTRODUCTION

The DR11-C is a general-purpose interface between the PDP-11 Unibus and a user's peripheral (Figure 1-1). The DR11-C provides the logic and buffer register necessary for program-controlled parallel transfers of 16-bit data between a PDP-11 System and an external device. The interface also includes status and control bits that may be controlled by either the program or the external device for command, monitoring, and interrupt functions. The DR11-C is software compatible with the DR11-A.

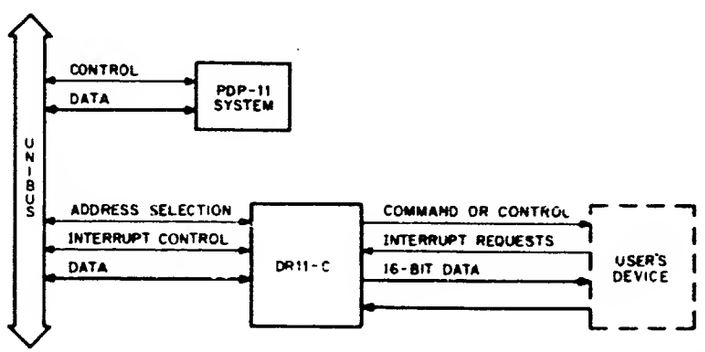

Figure 1-1 System Block Diagram

1.2 GENERAL DESCRIPTION

The DR11-C interface consists of three functional sections: address selection logic, interrupt control logic, and device interface logic.

The address selection logic determines if the interface has been selected for use, which register is to be used, if a word or byte operation is to be performed, and what type of transfer (input or output) is to be performed.

The interrupt control logic permits the interface to gain bus control and perform program interrupts to specific vector addresses. The interrupt enable bits are under program control; the interrupt bits are under control of the user's device.

The DR11-C interface logic consists of three registers: control and status, input buffer, and output buffer. Operation is initialized under program control by addressing the DR11-C to specify the register and the type of operation to be performed.

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If an output operation is specified, information from the Unibus is stored in a 16-bit register. Once this register has been loaded under program control (e.g., MOV R0, OUTBUF), the outputs are available to the device until the register is loaded with new data from the bus. The register can also be read onto the bus. Upon transfer of data to the buffer register, NEW DATA READY control signals are supplied to indicate to the user's device that data has been loaded by means of a DATO or DATOB bus cycle and is read by means of a DATI or DATIP bus cycle.

When an input operation is specified, the DR11-C provides 16 lines of input to Unibus transmitters. This permits data from the user's device to be read onto the bus. A control signal, DATA TRANSMITTED, informs the device that the input lines have been read. The input lines, which are not buffered, can be read by a DATI bus cycle (e.g., MOV INBUF, R0).

The control and status register provides six bits that can be used to control and monitor user functions. Two of these bits are interrupt enable (INT ENB) bits under control of the program. Two bits (REQ A and B) are under direct control of the user's device and can only be read by the program. These bits can be used either to initiate interrupt requests or to provide flags that can be monitored by the program. The remaining two bits (CSR0 and CSR1) are read/write bits that can be controlled by the program to provide command or monitoring functions. In the maintenance mode, they are also used to check operation of the interface.

A maintenance cable, which is supplied with the interface, permits checking of the DR11-C logic by loading the input buffer from the output buffer rather than from the user's device. Thus, a word from the bus is loaded into the output register and the same word appears when reading the input buffer, provided the interface is functioning properly.

The DR11-C can also be used as an interprocessor buffer (IPB) to allow two PDP-11 processors to transfer data between each other. In this case, one DR11-C is connected to each processor bus and the two DR11-Cs are cabled together, thereby permitting the two processors to communicate. A description of the DR11-C used as an interprocessor buffer is provided in Chapter 6. DEC does not supply software for this configuration.

1.3 PHYSICAL DESCRIPTION

The DR11-C interface is packaged on a single M7860 quad module that can easily be plugged into either a small peripheral slot in the processor or into one of the four slots in a DD11-A Peripheral Mounting Panel (Figure 1-2). Power is applied to the logic through the power harness already provided in the BA11 mounting box. The required current is approximately 1.5A at +5V. No -15V power source is needed.

The M7860 module has two Berg connectors for all user input/output signals. Two M971 connector boards, which are *not* supplied with each interface, can be used to bring all input/output lines to individual pins on a back panel via two BC08-R cables. Note that this cable is a "mirror image" rather than a straight one-to-one cable (Figure 3-1).

Specifications for the basic DR11-C are given in Table 1-1. The DR11-C interface is available in the following standard configuration:

a. one M7860 Interface module
b. one BC08R-1 Maintenance Cable
c. applicable documentation

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The following accessories are available for interfacing and may be ordered separately:

a. BC08R (Berg-to-Berg) flat cable. Available in lengths of 1, 6, 8 10, 12, 20, and 25 feet. When ordering, the dash number indicates the desired cable length; e.g., BC08R-1 or BC08R-25.

b. M971 connector board. A single-height by 8-1/2 in. board that brings the signals from one Berg connector to the module fingers.

c. H856 Berg connector. Includes an H856 Berg connector and 40 pins. Crimping tools are available from: Berg Electronics, Inc., New Cumberland, Pa. 17070.

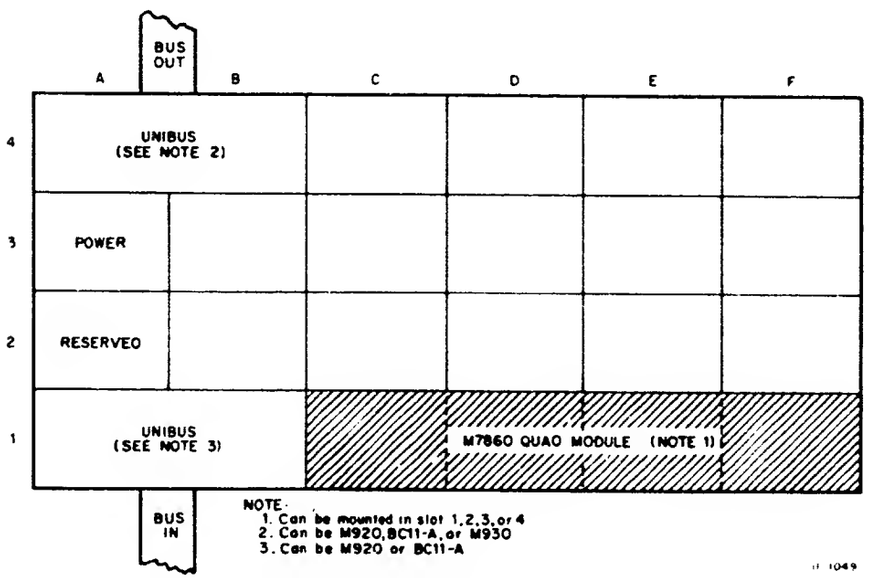

Figure 1-2 Typical M7860 Quad Module Mounting In a DD11-A

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Table 1-1
DR11-C Specifications

Registers	Status and Control Register (DRCSR) Output Buffer Register (DROUTBUF) Input Buffer Register (DRINBUF)
Register Addresses	DRCSR – 767770 DROUTBUF – 767772 DRINBUF – 767774 } may be changed by user
Interrupts	Priority = BR5 (may be changed by jumper plug) Vector = 300, 304 (user selectable) Types = REQUEST A, B (function defined by user)
Control and Status Bits	Controlled by program = INT ENB A, B; CSR0, CSR1 Controlled by device = REQUEST A,B
Inputs	One standard TTL unit load; diode protection clamps to ground and +5V
Outputs	TTL levels capable of driving 8 unit loads except for the following: NEW DATA READY = 30 unit loads DATA TRANSMITTED = 30 unit loads INIT (initialize) = common signal on both connectors driven by one 30-unit load driver
Signals	NEW DATA READY – drives 30 unit loads, positive pulse, 400-ns wide unless width changed by an external capacitor DATA TRANSMITTED – drives 30 unit loads, positive pulse, 400-ns wide unless width changed by an external capacitor INIT (initialize) – common signal on both connectors driven by one 30-unit load driver NEW DATA READY LO H – drives 30 unit loads, positive pulse, 400-ns wide unless width is changed by an external capacitor (only on etch revision F or later) NEW DATA READY HI H – drives 30 unit loads, positive pulse, 400-ns wide unless width is changed by an external capacitor (only on etch revision F or later)
Data Inputs	16-bit word from the external device
Data Outputs	16-bit word from the Unibus. Either a full word or an 8-bit byte (either high or low) may be loaded from the bus.
Maintenance Mode	A MAINT cable (supplied with basic system) jumpers the DROUTBUF outputs to the DRINBUF inputs and forces bits 15 and 07 to read as CSR1 and CSR0, respectively.
Size	Consists of a single quad module (M
Mounting	M7860 module occupies 1/4 of a DD11-A (or equivalent) or one of two controller slots in a KA11, KC11, or other PDP-11 processor system unit.
Power	≈1.5A @ +5V (derived from power supply in mounting box where DR11-C is installed)

CHAPTER 2
SOFTWARE INTERFACE

2.1 SCOPE

This chapter presents a detailed description of the three DR11-C registers (Figure 2-1). These registers are assigned bus addresses and can be read or loaded (with the exceptions noted) using any instruction that refers to their addresses. The mnemonic INIT refers to the initialization signal issued by the processor. Initialization is caused by one of the following: issuing a programmed RESET instruction; depressing the START switch on the processor console; or the occurrence of a power-up or power-down condition of a system power supply.

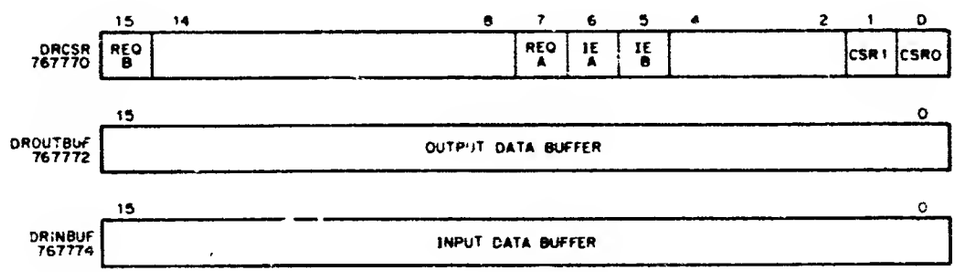

Figure 2-1 DR11-C Register Assignments

The device registers and associated addresses are listed in Table 2-1. Note that these addresses can be changed by altering the jumpers on the address selection logic. However, any programs or other software referring to these addresses must also be modified accordingly if the jumpers are changed. Paragraph 2.5 discusses priority levels and the addressing scheme when more than one DR11-C is used.

Table 2-1
Standard DR11-C Register Assignments

Register	Mnemonic*	Address
Control and Status Register	DRCSR	767770
Output Buffer	DROUTBUF	767772
Input Buffer	DRINBUF	767774

* First two letters of mnemonic (DR) refer to DR11-C interface, the remaining letters represent the mnemonic of a specific register.

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Paragraphs 2.2 through 2.4 describe operation of the DR11-C registers. Note that unused bits are always read as 0s. Loading unused or read-only bits has no effect on the bit position.

2.2 INPUT BUFFER REGISTER (DRINBUF)

The input buffer is a 16-bit read-only register that receives data from the user's device for transmission to the Unibus. Information to be read is provided by the user's device on the data IN signal lines. Because the input buffer consists of gating logic rather than a flip-flop register, the data IN lines must be held until read onto the bus. The register is read by a DATI sequence and the data is transmitted on the Unibus for transfer to the processor or some other device. When the input lines are read during a DATI sequence, a pulsed signal (DATA TRANSMITTED) is sent to the user's device to inform it that the transfer has been completed. The trailing edge of the positive-going pulse indicates that this transfer is completed.

Whenever the maintenance cable is used, the input buffer register receives data from the output buffer register rather than from the user's device. This permits checking of the interface logic by loading a word from the bus into the output register and verifying that the same word appears in the input buffer.

2.3 OUTPUT BUFFER REGISTER (DROUTBUF)

The output buffer is a 16-bit read/write register that may be read or loaded from the Unibus. Information from the bus is loaded into this register under program control. At the time of loading, pulsed signals (NEW DATA READY) are generated to inform the user's device that the register has been loaded. The trailing edge of the positive pulse should be used to allow the data to be loaded and settle on the user's input lines. Data from the buffer is transmitted to the user's device on the data OUT lines by means of a DATO or DATOB bus cycle.

The contents of the output buffer register may be read at any time by means of a DATI or DATIP bus cycle. During the read operation, the output of the buffer is fed directly to the bus data lines.

Whenever the maintenance cable is used, the data from the output buffer is also applied to the input buffer register. This permits checking operation of the interface logic.

The DROUTBUF is cleared by INIT.

2.4 CONTROL AND STATUS REGISTER (DRCSR)

The control and status register is used to enable interrupt logic and to provide user-defined command and status functions for the external device.

Two REQUEST bits, which are under device control, may be used to provide device status indications, or may be used to initiate interrupts when used with associated INT (interrupt enable) bits which are under program control. Two other bits (CSR0 and CSR1) are controlled from the Unibus and serve as command bits.

Although the REQUEST and CSR bits can be used for any function the user desires, standard PDP-11 interface conventions attempt to allocate bit 15 for error conditions and bit 07 for ready indications and both of these bits can generate interrupt requests. In addition, bit 00 is normally used for start or go commands.

Table 2-2 gives the bit assignments and provides a brief description of each bit in the control and status register.

2.5 ADDRESS AND VECTOR ASSIGNMENTS

The register address and vector address assignments are listed in Table 2-3. Note that four addresses are allotted for each DR11-C even though only three addresses are used.

Table 2-2
DRCSR Bit Assignments

Bit	Name	Meaning and Operation
15	REQUEST B	This bit is under control of the user's device and may be used to initiate an interrupt sequence or to generate a flag that may be tested by the program. When used as an interrupt request, it is set by the external device and initiates an interrupt provided the INT ENB B bit (bit 05) is also set. When used as a flag, this bit can be read by the program to monitor external device status. When the maintenance cable is used, the state of this bit is dependent on the state of CSR1 (bit 01). This permits checking interface operation by loading a 0 or 1 into CSR1 and then verifying that REQUEST B is the same value. Read-only bit. Cleared by INIT.
14–08	Unused	Not Applicable
07	REQUEST A	Performs the same function as REQUEST B (bit 15) except that an interrupt is generated only if INT ENB A (bit 06) is also set. When the maintenance cable is used, the state of REQUEST A is identical to that of CSR0 (bit 00). Read only bit. Cleared by INIT.
06	INT ENB A	Interrupt enable bit. When set, allows an interrupt sequence to be initiated, provided REQUEST A (bit 07) becomes set. Can be loaded or read by the program (read/write bit). Cleared by INIT.
05	INT ENB B	Interrupt enable bit. When set, allows an interrupt sequence to be initiated, provided REQUEST B (bit 15) becomes set. Can be loaded or read by the program (read/write bit). Cleared by INIT.
04–02	Unused	Not Applicable
01	CSR1	This bit can be loaded or read (under program control) from the Unibus and can be used for a user-defined command to the device (appears only on Connector No. 1). When the maintenance cable is used, setting or clearing this bit causes an identical state in bit 15 (REQUEST B). This permits checking operation of bit 15 which cannot be loaded by the program. Read/write bit (can be loaded or read by the program). Cleared by INIT.
00	CSR0	Performs the same function as CSR1 (bit 01) but appears only on Connector No. 2. When the maintenance cable is used, the state of this bit controls the state of bit 07 (REQUEST A). Read/write bit. Cleared by INIT.

Table 2-3
Address Assignments

No. of DR11-Cs	Register Addresses	Vector Addresses
DR11-C No. 0	767776 767770	300, 304
DR11-C No. 1	767766 767760	310, 314
DR11-C No. 2	767756 767750	320, 324
.	.	.
.	.	.
.	.	.
DR11-C No. 7	767706 767700	370, 374
.	.	.
.	.	.
.	.	.
DR11-C No. 15	767606 767600	470, 474

The addresses in the above table were assigned assuming that the system contains only DR11-Cs and no DR11-As. If DR11-A interfaces are present in the system, addresses must be assigned for them before assigning DR11-C addresses.

The DR11-C has floating vectors which are assigned in the following sequence

a. Starting at 300 and proceeding upward, assign all DC11s
b. Then any extra KL11s called for (VT05, VT06, LC11).
c. Then any DP11s
d. Then any DM11s
e. Then any DN11s
f. Then any DM11-BBs
g. Then any DR11-As
h. Then any DR11-Cs

NOTE
Some devices use only one vector address.

The register address and vector address assignments are implemented by changing jumpers on the M7860 module. The register address lines are jumpered for a 0; the vector address lines are jumpered for a 1. A more detailed explanation of these jumpers is given in Chapter 4 of this manual.

The priority level of both interrupts must be the same, with interrupt A (REQUEST A) on a higher sublevel than interrupt B (REQUEST B). REQUEST A uses the vector block with the least significant octal digit equal to 0 (i.e., REQUEST B uses the vector block with the least significant octal digit equal to 4 (i.e., REQUEST A using 430 and REQUEST B using 434). The M7860 module contains a priority jumper plug which is normally set at the BR5 level. This priority level may be changed by changing the jumper plug. (Levels of BR4 through BR7 are available.)

Direct memory access (NPR request) is not possible with a DR11-C interface.

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CHAPTER 3
USER INPUT/OUTPUT SIGNALS

3.1 SIGNAL LIST

Tables 3-1 and 3-2 list the signals available to the user's device. Input loading refers to the number of TTL unit loads the input signal must drive. A unit load is defined as:

2.4V ≤ Input high voltage ≤ 5.0V @ 40 μA
0.0V ≤ Input low voltage ≤ 0.4V @ -1.6 mA

where current flow is defined as positive into the driven gate. All inputs are one standard TTL unit load and have diode protection clamps to ground and +5V.

Table 3-1
User Input Signals

Name	No. of Signals	Loading	Description
IN00 through IN15	16	1 each	Data input from user device. The levels presented on these lines can be examined by reading the input buffer register (DRINBUF) with an instruction such as MOV DRINBUF, R0. This data is transferred to the Unibus when the DR11-C responds to a DATI bus cycle. Because the input buffer register consists of gating logic, the device must hold the IN lines asserted until read onto the Unibus. This is indicated by the trailing edge of the DATA TRANSMITTED pulse. Logic levels are: +3V = 1; 0V = 0.
REQUEST A, B	2	1 each	Two request lines that can be asserted (+3V) by the external device to initiate an interrupt sequence or to generate a flag that can be tested by the program. These request lines must be levels that are held asserted for the entire interrupt sequence and would normally be cleared by NEW DATA READY or DATA TRANSMITTED. Although the external device controls these request lines, an interrupt sequence can only be started by the program because of the associated interrupt enable (IE) bits under program control. Methods of generating these request levels in the user's device are described in Chapter 6. Logic levels are: +3V = 1, 0V = 0.

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Table 3-2
User Output Signals

Name	No. of Signals	Driving Capability	Description
OUT00 through OUT15	16	7 each	Data output to user's device. These signals represent the contents of the output buffer register (DROUTBUF), which is loaded under program control (e.g., MOV R0, DROUTBUF). Logic levels are: +3V = 1, 0V = 0. All lines are cleared to 0 by INIT.
NEW DATA READY	1	30	This pulsed signal is generated when either byte of the DROUTBUF is loaded to indicate to the user's device that the buffer is loaded with data from the Unibus. The signal is true (+3V) as soon as the DROUTBUF has been addressed for loading and remains true for approximately 400 ns; therefore, the trailing edge of this pulse should be used for sampling the lines at the user's end of the cable. This duration can be changed as described in Paragraph 3.2.
NEW DATA READY LO	1	30	This pulsed signal is only generated when the low byte of the DROUTBUF is loaded. The signal is only available on M7860 modules of etch revision F or later. Otherwise, the description for NEW DATA READY applies.
NEW DATA READY HI	1	30	This pulsed signal is only generated when the high byte of the DROUTBUF is loaded. The signal is only available on M7860 modules of etch revision F or later. Otherwise, the description for NEW DATA READY applies.
DATA TRANSMITTED	1	30	This pulsed signal is generated when the DRINBUF register is read by a DATI sequence to inform the user's device that the transfer has been completed. The signal is true (+3V) as soon as the DRINBUF has been addressed for reading and remains true for approximately 400 ns; therefore, the lines should be held until the trailing edge of this signal. This duration can be changed by the user as described in Paragraph 3.2.
CSR0, 1	2	7 each	Device status bits 0 and 1. The levels applied to these lines appear as bits 00 and 01 in the control and status register (DRCSR). These two lines can be loaded or read from the Unibus (under program control). When the DR11-C is used as an interprocessor buffer, these bits are used for communication between the two processors. Logic levels are: +3V = 1, 0V = 0 Cleared by INIT.
INIT	1	30 (one driver for the signal on both of the cables)	This line is true (+3V) whenever the Unibus is initialized, which occurs during any one of the following conditions: a programmed RESET instruction is issued, the console START switch is depressed, or a power-up or power-down condition occurs.

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All outputs are TTL levels capable of driving seven unit loads with the following exceptions:

NEW DATA READY - 30 unit loads
NEW DATA READY LO - 30 unit loads
NEW DATA READY HI 30 unit loads
DATA TRANSMITTED - 30 unit loads
INIT - a common signal on both connectors which is driven by one 30-unit load driver

The NEW DATA READY and DATA TRANSMITTED signals are described more fully in Paragraph 3.2.

3.2 VARIABLE SIGNALS

The NEW DATA READY signals are positive pulses which load the output buffer register on the leading edge of the pulse. The DATA TRANSMITTED signal is also a positive pulse and is generated when the input buffer register is read by a DATI sequence.

Both of these signals are approximately 400 ns in duration. However, this duration can be changed by adding an external capacitor between back panel pin EB1 and ground. Some typical capacitor values and resultant pulse widths are listed in Table 3-3. The effect of the additional capacitance results in lengthening the bus cycle. This is, therefore, a factor in NPR latency considerations.

Table 3-3
External Capacitor Values

External Capacitor	NEW DATA READY	DATA TRANSMITTED
none	350 ns	450 ns
470 pF	50[illegible] ns	600 ns
820 pF	[illegible]0 ns	750 ns

3.3 CONNECTORS

Figure 3-1 illustrates the layout for the M7860 module, the Berg connectors, and the M971 connector modules referenced in Tables 3-4 and 3-5.

The input and output signals are listed in Table 3-4 and indicate the Berg pin on the M7860 module. Table 3-5 lists all pin connections (in pin number order) for the Berg header on the M7860 module, the Berg header on the M971, and the M971 board pins. Figure 3-2 illustrates the physical location of the pins on the Berg connector.

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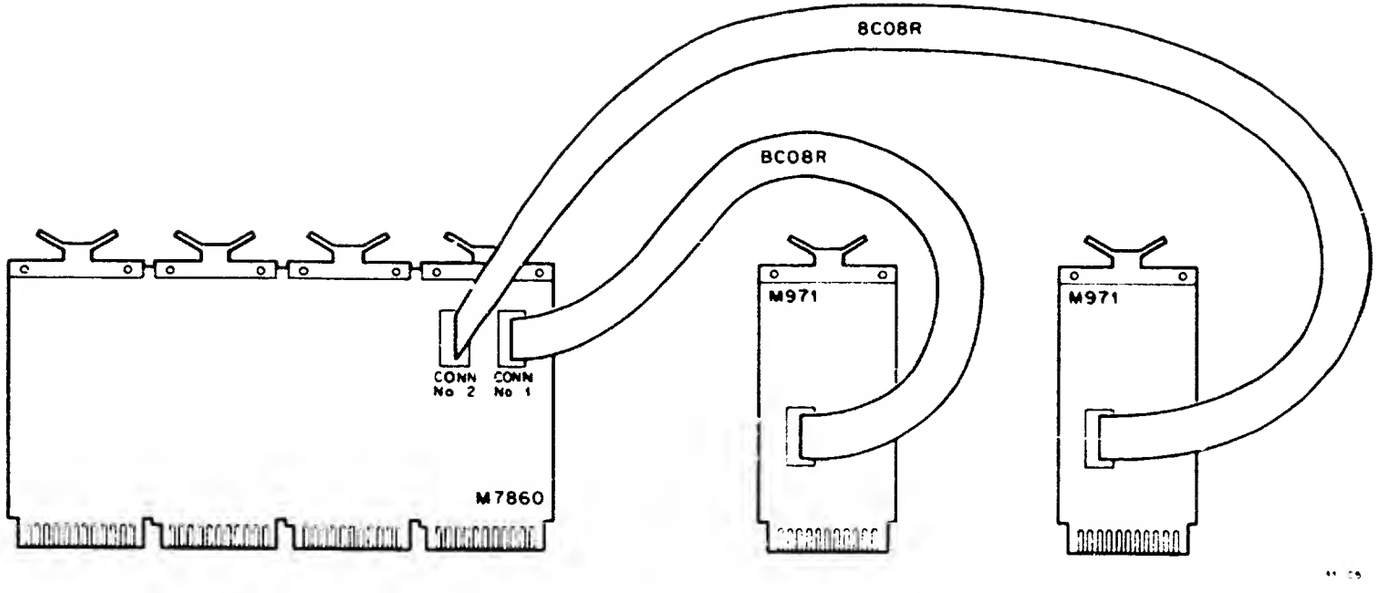

Figure 3-1 M7860 Module Interconnect Diagram
When The Optional M971 Connectors Are Used.

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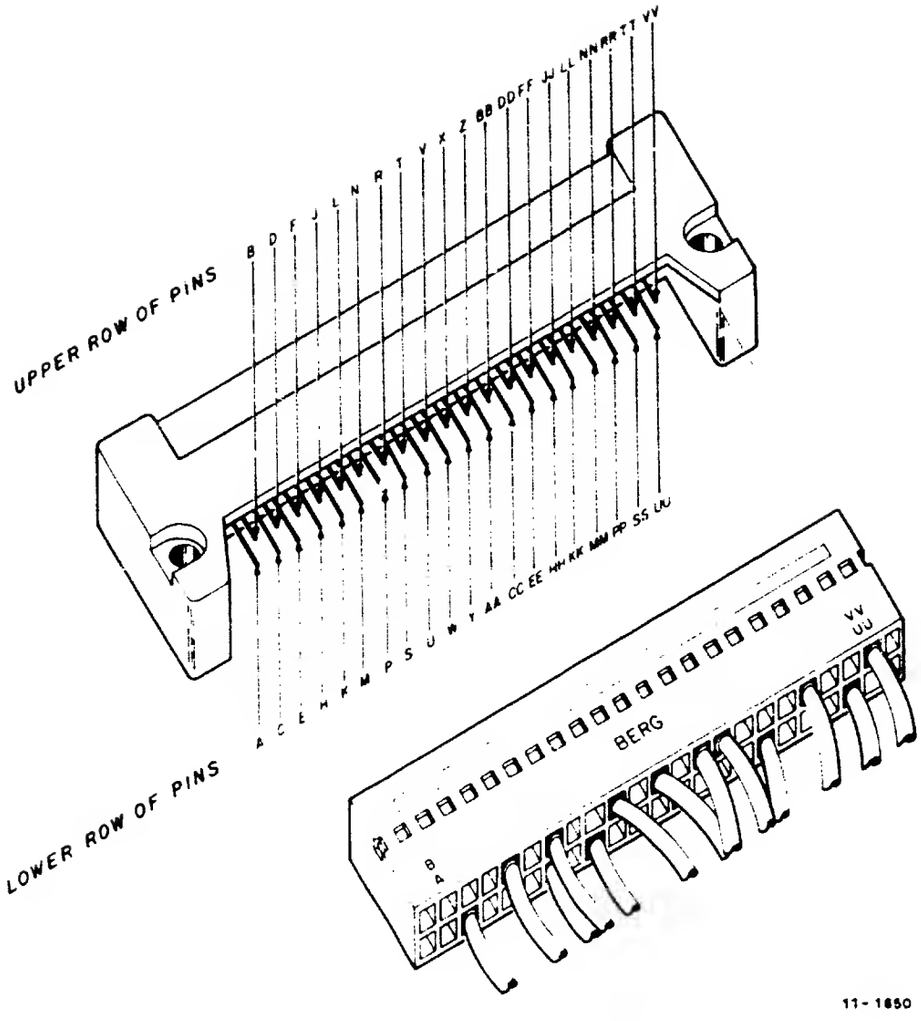

Figure 3-2 Berg Connector

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Table 3-4
Input and Output Signals

Inputs			Outputs		
Signal	Connector	Pin	Signal	Connector	Pin
IN00	2	TT	OUT00	1	C
IN01	2	LL	OUT01	1	K
IN02	2	H	OUT02	1	NN
IN03	2	BB	OUT03	1	U
IN04	2	KK	OUT04	1	L
IN05	2	HH	OUT05	1	N
IN06	2	EE	OUT06	1	R
IN07	2	CC	OUT07	1	T
IN08	2	Z	OUT08	1	W
IN09	2	Y	OUT09	1	X
IN10	2	W	OUT10	1	Z
IN11	2	V	OUT11	1	AA
IN12	2	U	OUT12	1	BB
IN13	2	P	OUT13	1	FF
IN14	2	N	OUT14	1	HH
IN15	2	M	OUT15	1	JJ
REQ A	1	LL	NEW DATA RDY*	1	VV
REQ B	2	S	DATA TRANS.*	2	C
			CSR0	2	K
			CSR1	1	DD
			INIT	1	P
			INIT	2	RR, NN

* Pulse signals, approximately 400-ns wide. Width can be changed by user.

Table 3-5
Pin Connections

M971		M7860				M971	
		Connector No. 2		Connector No. 1			
Board	Berg Header	Pin	Name	Name	Pin	Berg Header	Board
V2	A	VV	OPEN	OPEN	A	VV	A1
U1	B	UU	GND	OPEN	B	UU	A2
U2	C	TT	IN00	OUT00	C	TT	A1
V1	D	SS	GND	OPEN	D	SS	A2
T2	E	RR	INIT H	NEW DATA RDY III	E	RR	B1
T1	F	PP	GND	OPEN	F	PP	B2
T2	H	NN	INIT H	NEW DATA RDY I O	H	NN	C1
T1	J	MM	GND	GND	J	MM	C2
S2	K	LL	IN01	OUT01	K	LL	D1
S1	L	KK	IN04	OUT04	L	KK	D2
R2	M	JJ	GND	GND	M	JJ	E1
R1	N	HH	IN05	OUT05	N	HH	E2
P2	P	FF	OPEN	INIT H	P	FF	E1

(continued on next page)

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Table 3-5 (Cont)
Pin Connections

M971		M7860				M971	
Board	Berg Header	Connector No. 2 Pin	Name	Name	Connector No. 1 Pin	Berg Header	Board
P1	R	EE	IN06	OUT06	R	EE	F2
N2	S	DD	GND	GND	S	DD	H1
N1	T	CC	IN07	OUT07	T	CC	H2
M2	U	BB	IN03	OUT03	U	BB	J1
M1	V	AA	GND	GND	V	AA	J2
L2	W	Z	IN08	OUT08	W	Z	K1
L1	X	Y	IN09	OUT09	X	Y	K2
K2	Y	X	GND	GND	Y	X	L1
K1	Z	W	IN10	OUT10	Z	W	L2
J2	AA	V	IN11	OUT11	AA	V	M1
J1	BB	U	IN12	OUT12	BB	U	M2
H2	CC	T	GND	GND	CC	T	N1
H1	DD	S	REQ B	CSR1	DD	S	N2
F2	EE	R	GND	GND	EE	R	P1
F1	FF	P	IN13	OUT13	FF	P	P2
E2	HH	N	IN14	OUT14	HH	N	R1
E1	JJ	M	IN15	OUT15	JJ	M	R2
D2	KK	L	GND	GND	KK	L	S1
D1	LL	K	CSR0	REQ A	LL	K	S2
C2	MM	J	GND	GND	MM	J	T1
C1	NN	H	IN02	OUT02	NN	H	T2
B2	PP	F	OPEN	GND	PP	F	T1
B1	RR	E	OPEN	OPEN	RR	E	T2
A2	SS	D	OPEN	GND	SS	D	V1
A1	TT	C	DATA TRANS.	OPEN	TT	C	U2
A2	UU	B	OPEN	GND	UU	B	U1
A1	VV	A	OPEN	NEW DATA RDY	VV	A	V2

I2

CHAPTER 4
THEORY OF OPERATION

4.1 INTRODUCTION

This chapter provides a detailed description of the DR11-C interface. The interface may be divided into five major functional areas: selection logic, interrupt logic, status register, input buffer register, and output buffer register. A block diagram of the DR11-C is shown in Figure 4-1. Each of the functional areas is covered separately in subsequent paragraphs. The basic purpose of each of these areas is as follows:

Selection Logic	Determines if the DR11-C interface has been selected for use, which register is to be used, if a byte or word operation is required, and what type of transfer (DATI or DATO) is to be performed.
Interrupt Logic	Permits the DR11-C to gain bus control and perform a program interrupt. Priority level of bus request (BR) line may be changed by the user.
Status Register	A 16-bit register used to provide user-defined command and monitoring functions; includes interrupt enable bits. Four bits are under program control, two are under device control. Some of the bits in this register can be used for communication if the DR11-C is part of an interprocessor buffer.
Input Buffer Register	A 16-bit read-only buffer that receives data from the user's device for transmission to the Unibus.
Output Buffer Register	A 16-bit read/write register that can be loaded or read from the Unibus. Once the buffer has been loaded, the data is available for transfer to the user's device.

4.2 ADDRESS SELECTION

The address selection logic (drawing DR-4) decodes the incoming address information from the bus and provides four select line (three used) and three gating signals that determine which register has been selected and whether it is to perform an input or output function. Jumpers on the logic are arranged so that the module responds only to standard device register addresses 767770, 767772, 767774, and 767776 (jumper in bit position 12). Although these addresses have been selected by DEC as the standard assignments for the DR11-C interface, the user may change the jumpers to any address desired. However, any MainDEC program (or other software) that references the DR11-C standard address assignments must also be modified if other than the standard assignments are used.

The first five octal digits of the address (76777) indicate that the DR11-C has been selected as the device to be used. The final octal digit, consisting of address lines A02, A01, and A00, determines which register has been selected and whether a word or byte operation is to be performed. The two mode control lines, C1 and C0, determine whether the selected register is to perform an input or output function.

K2

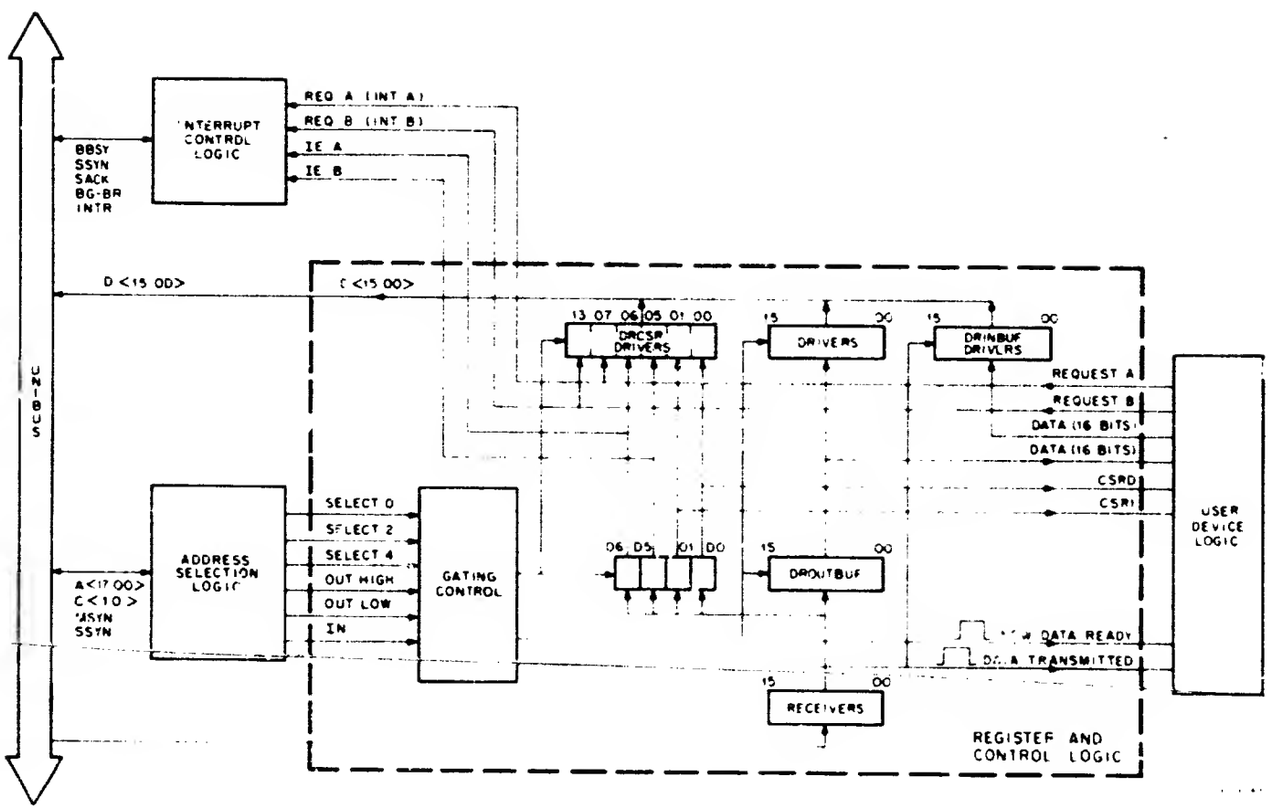


Figure 4-1 DR11-C Interface, Block Diagram

Address lines A02 and A01 are decoded to produce one of four select line signals (Table 4-1) which select the register to be used. The two mode control lines produce IN and OUT gating signals (Table 4-1) which determine whether the bus cycle is a DATI or DATO. Note that an IN gating signal is provided for all three registers because all three can be read from the bus. However, an OUT gating signal is not provided for the input buffer register because it cannot be loaded from the bus.

Table 4-1
Gating and Select Line Signals

Select Line	Gating Signal	Function Selected	Reg.	Bus Cycle
0	IN	status to bus	DRCSR	DATI
2	IN	output buffer to bus	DROUTBUF	DATI
4	IN	input buffer to bus	DRINBUF	DATI
0	OUT LOW	bus to status	DRCSR	DATOB
0*	OUT HIGH	unused	–	DATOB
2	OUT LOW, OUT HIGH	bus to output buffer	DROUTBUF	DATO or DATOB
4*	OUT LOW, OUT HIGH	unused	–	DATO or DATOB
6*	IN or OUT	unused	–	DATI, DATO, or DATOB

* Executing any of the above operations referred to as unused does not result in an error trap or any other bus indication. The function is simply not performed.

There are two OUT signals, OUT LOW and OUT HIGH, that refer to the low and high byte of a register, respectively. Both OUT LOW and OUT HIGH are provided for the output buffer register which can be loaded with a full word from the bus. Only OUT LOW, however, is provided for the status register because the high byte contains no bits which can be written into.

The basic functions of the IN and OUT signals are:

a. IN – DR11-C responds by placing data from the selected register onto the bus.
b. OUT LOW – DR11-C loads low byte of selected register.
c. OUT HIGH – DR11-C loads high byte of selected register.

Note that both OUT LOW and OUT HIGH are active when a full 16-bit word is being loaded into a register.

4.2.1 Inputs

A simplified block diagram of the address selection logic is shown in Figure 4-2. Note that IN and OUT are always used with respect to the master (controlling) device. Thus, when the DR11-C interface is used, an OUT transfer is a transfer of data out of the master (usually the processor) and into the device. Similarly, an IN transfer is the operation of the interface furnishing data to the Unibus.

m2

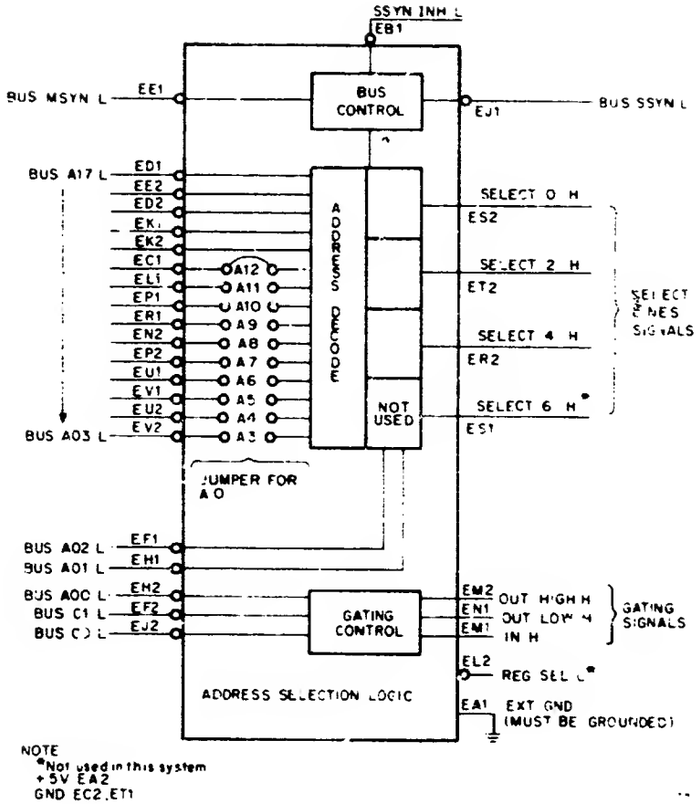


Figure 4-2 Address Selection Logic, Simplified Diagram

The address selection logic input signals consist of 18 address lines, A(17:00); 2 bus control lines, C(1:0); and a master synchronization (MSYN) line. The address selection logic decodes the incoming address as described below. This address format is shown in Figure 4-3. Note that all input gates are standard bus receivers.

a. Line A00 is used for byte control.

b. Lines A01 and A02 are decoded to select one of the four addressable device registers (only three are used).

c. Decoding of lines A(12:03) is determined by jumpers. When a given line contains a jumper, the address logic searches for a 0 on that line. If there is no jumper, the logic searches for a 1.

NOTE

Connection of jumpers on the M7860 quad module is identical to the method used on the M105 Address Selector module used in other interfaces.

d. Address lines A(17:13) must be all 1s. This specifies an address within the top 8K byte address bounds for device registers.

CAUTION

Pin EA1 (EXT.GND) must be grounded by the user to ensure proper operation of the address selection logic.

A3

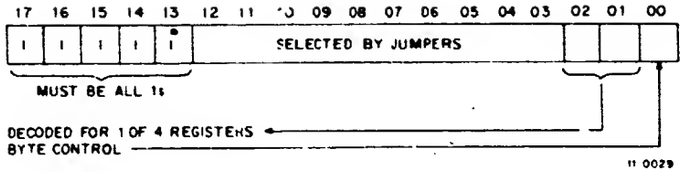


Figure 4-3 Interface Select Address Format

4.2.2 Outputs

The address selection logic output signals are used to permit selection of three 16-bit registers and provide three signals used for gating information into and out of the master device. All of these output signals are listed in Table 4-1. Note that the logic diagram (drawing DR-4) shows an additional select line signal, SELECT 6. This particular signal is not used by the DR11-C interface but the interface can respond to that address

Tables 4-2 and 4-3 indicate the input signals that select the control output line states.

Table 4-2
Select Lines

Input Lines A(02:01)	Select Lines True (+3V)
00	0
01	2
10	4
11	6 (not used)

NOTES: 1. Lines A(17:13) must be all 1s (0V on Unibus).

2. Lines A(12:03) are selected by jumpers.

Table 4-3
Gating Control Signals

Mode Control C(1:0)	Byte Control A00	Gating Control Signals True (+3V)	Bus Sequence
00	0	IN	DATI
00	1	IN	DATI
01	0	IN	DATIP
01	1	IN	DATIP
10	0	OUT LOW OUT HIGH	DATO
10	1	OUT LOW OUT HIGH	DATO
11	0	OUT LOW	DATOB
11	1	OUT HIGH	DATOB

NOTE: Gating control signals may become true although select lines are not

4.2.3 Slave Sync (SSYN)

The SSYN INH signal is supplied without an external capacitor and SSYN is returned to the master approximately 400 ns after interface selection. Because MSYN is used to produce both SSYN and the SELECT line signals, which in turn produce the DR11-C control signals, an external capacitor can be added at pin FB1 to change the duration of NEW DATA READY and DATA TRANSMITTED. Typical capacitor values and durations are listed in Table 3-3. If SSYN INH is grounded, it inhibits the acknowledgment signal (SSYN) which must then be generated by another source.

4.3 INTERRUPT CONTROL

The interrupt control logic (drawing DR-4) permits the DR11-C interface to gain control of the bus (become bus master) and perform an interrupt operation. The jumpers on this logic can be arranged so that a vector address can be assigned according to the method described in Paragraph 2.5. Although this is the recommended method of assigning vector addresses, the user may change the jumpers to correspond to any address desired, but MainDEC programs and other software referencing these standard vector address assignments must also be changed to reflect the new addresses.

NOTE

Connection of jumpers on the M7860 quad module is the *reverse* of the method used on M782 and M7820 Interrupt Control modules and is the same as that used on the M7821 module. On the M7860 quad module, a jumper represents a 1, no jumper represents a 0.

The interrupt control logic consists of a dual input request and grant acknowledge circuit for establishing bus control. The A input is connected to the REQUEST A control logic and provides a vector address of 300, the B input is connected to the REQUEST B logic and provides a vector address of 304.

Before the A input interrupt logic can generate an interrupt request, two input signals must be high: REQUEST A and INT ENB A. The logic that generates these two signals is shown on drawing DR-3. When a 1 is loaded into bit 06 of the status register (DRCSR), it sets the INT ENB A flip-flop to produce INT ENB A H. This signal is applied to the interrupt control logic as an enabling signal.

NOTE

The status register bits function as individual flip-flops but are physically part of an 8271 IC chip. In subsequent discussions, each bit is treated as a single flip-flop. Schematics of the 8271 IC are given in Appendix A.

The second signal that must be present to generate an interrupt sequence is REQUEST A H. This signal must be produced in the user's device as described in Chapter 6 of this manual.

The A input section of the interrupt logic (Figure 4-4) is used to gain control of the bus when both the REQUEST A and INT ENB A inputs are asserted. A bus request is made on the BR level corresponding to the level of the priority plug in the logic.

The standard level for the DR11-C interface is BR5, but this may be changed on the priority plug if desired. When the priority arbitration logic in the processor recognizes the request and issues a bus grant signal, the master control circuit acknowledges with a SACK signal. When the DR11-C interface has fulfilled all requirements to become bus master (BBSY false, SSYN false, and BG false), the master control section asserts BBSY.

C3

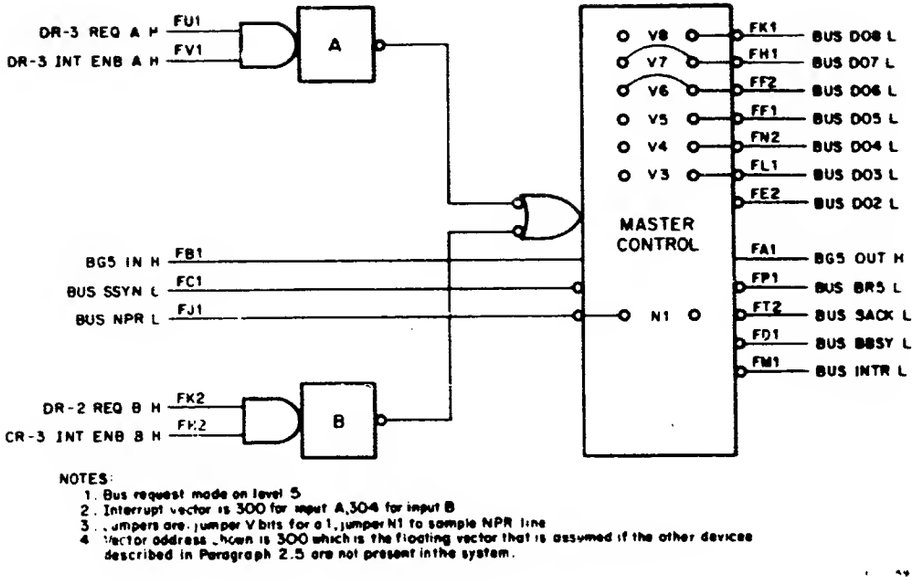


Figure 4-4 Interrupt Control Logic, Simplified Block Diagram

The B input interrupt logic operates in a similar manner to that of the A input logic. In this case, the two input signals that must be high are: REQUEST B and INT ENB B. The logic for INT ENB B is shown on drawing DR-3. When a 1 is loaded into bit 05 of the status register (DRCSR), it sets the interrupt flip-flop to produce INT ENB B H which is applied to the interrupt logic as an enabling signal.

The second signal that must be present is REQUEST B H. As shown on drawing DR-2, this signal must also be produced in the user's device as described in Chapter 6 of this manual.

The B input interrupt logic functions in an identical manner to the A input logic except that it generates a different vector address. Although both REQUEST A and REQUEST B are at a BR5 level, REQUEST A has a slightly higher priority.

Once the DR11-C interface has gained bus control by means of a BR request, an interrupt is generated. The interrupt vector address is selected by jumpers on the logic as shown in Figure 4-4. Because the vector is a 2-word (4-byte) block, it is not necessary to assert the state of bits 0 and 1.

The six selectable (jumpered) lines determine the two most significant octal digits of the vector address. The least significant octal digit is controlled by bit 02 so that all vector addresses end in either 0 or 4. The input to bit 02 is tied to the V2 flip-flop logic. Whenever an interrupt occurs on input A, bus line D02 is *not* asserted, and the interrupt causes a vector at location 300. When a B input interrupt occurs, bus line D02 is asserted, and the interrupt causes a vector at location 304. Note that the first two octal digits can be changed by jumpers but the last octal digit is always 0 or 4.

The BG IN signal is allowed to pass through the logic to BUS BG OUT when the interface is not issuing a request. To request bus use, the AND condition of REQUEST and INT ENB must be satisfied. These levels must be true until the interrupt service routine clears REQUEST or INT ENB. Once bus control has been attained, it is released when the processor responds with BUS SSYN after it has strobed in the interrupt vector. After releasing bus control, the logic inhibits further bus requests from that input (A or B) even if REQUEST and INT ENB

D3

remain asserted. In order to make another bus request, REQUEST or INT ENB must be dropped and then re-asserted to cause the logic to reassert the request line. This prevents multiple interrupts when the master control is used to generate interrupts.

Note that the interrupt control logic used in the DR11-C interface is not capable of issuing NPR requests. To improve NPR latency, the NPR line is sampled and prevents completion of an interrupt sequence until all NPRs have been honored. The sampling of the NPR line is controlled by a jumper (N1) on the M7860 module.

CAUTION

Only certain PDP-11 processors can work with the special circuit described above. The jumper (N1) on the M7860 module, when cut, prevents this special circuit from working.

4.4 CONTROL AND STATUS REGISTER (DRCSR)

The control and status register is used to provide user-defined commands for the external device and to monitor operation of the external device. The status register is a 16-bit register, of which six bits are used.

Four of the status register bits (bits 00, 01, 05, and 06) are read/write bits under program control. Each of these bits functions as an individual flip-flop but all four are physically part of a single 8271 IC chip. In subsequent discussions, each bit is referred to as a single flip-flop; however, on the logic drawing (DR-3) they are shown as an 8271 IC. Detailed schematics of the 8271 IC are given in Appendix A. Note that the IC is normally used as a 4-bit shift register, but in this instance, the shift input is disabled (grounded).

Four of the six status register bits (00, 01, 05, and 06) can be read or loaded from the bus. This read/write capability is accomplished by the input/output gating logic shown on drawing DR-3. A simplified version of this gating is shown in Figure 4-5 and described below. The figure illustrates the gating for a single bit (bit 06); however, the other three bits function in a similar manner.

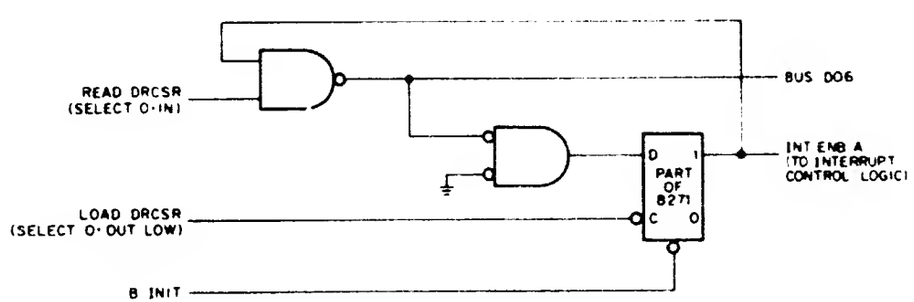


Figure 4-5 Status Register Input/Output Gating (one bit position)

When the status register is addressed for reading, the SELECT 0 and IN signals become true and gate the output of the flip-flop to bus data line D06 for reading.

If it is desired to load the DRCSR, the appropriate level is placed on bus line BUS D06 and serves as the data input to the flip-flop. The clock input becomes true when the DRCSR is addressed for loading (SELECT 0 and OUT LOW are both true)

E3

The outputs of the bit 05 and 06 flip-flops (INT ENB A, B) are applied as an enabling level to the interrupt control logic described in Paragraph 4.3.

The outputs of the bit 00 and 01 flip-flops (CSR0 and CSR1) are available to the user and, if desired, can be used as commands to initiate operations within the external device.

It should be noted that all of the read/write status register bits are located in the low-order byte. Therefore, byte addressing can be used for access to these bits. When reading, word addressing must be used if it is desired to read all six bits. However, in the case of loading the register, only DATOB bus cycles are required because any bit that can be loaded from the bus is in the low-order byte of the register.

The remaining two status register bits (07 and 15) are read-only bits which are generated by the external device as described in Chapter 6 of this manual. The logic for these bits (REQUEST A, B) is shown on drawings DR-3 and DR-2, respectively. A simplified version of the logic is shown in Figure 4-6 and described below.

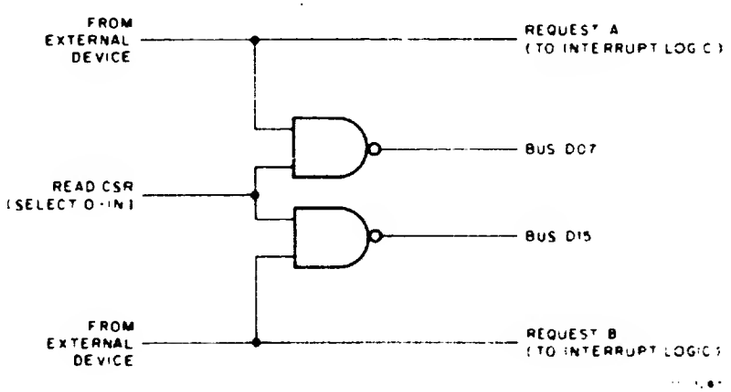


Figure 4-6 DRCSR Read-Only Bits (REQUEST A and B)

When the external device generates a REQUEST level, it is applied directly to the interrupt control logic to initiate an interrupt sequence, provided the associated INT ENB bit has been set. If it is desired to use the REQUEST level as a flag rather than for an interrupt request, then the INT ENB bit is not set by the program and the REQUEST line is read by the program. During this read operation, READ CSR is true and gates the REQUEST level to the appropriate bus data line for reading.

The CSR0 and CSR1 bits and the two REQUEST bits can be used for communication between interfaces when two DR11-C units are being used as an interprocessor buffer. For example, the CSR0 bit in one interface is connected to the REQUEST A input line of the second interface. If the program then sets CSR0 in the first interface, REQUEST A is true in the second interface which then initiates an interrupt sequence. A discussion of the DR11-C used as an interprocessor buffer is covered in Chapter 6 of this manual.

4.5 OUTPUT BUFFER REGISTER (DROUTBUF)

The output buffer is a 16-bit read/write register that can be read or loaded from the Unibus. This register consists of four 82 11 IC chips and associated input/output gating. The register logic is shown on drawings DR-2 and DR-3. A simplified version of the DROUTBUF logic is shown in Figure 4-7 and described below. This figure illustrates a single register bit (bit 03). All other bits function in an identical manner.

F3

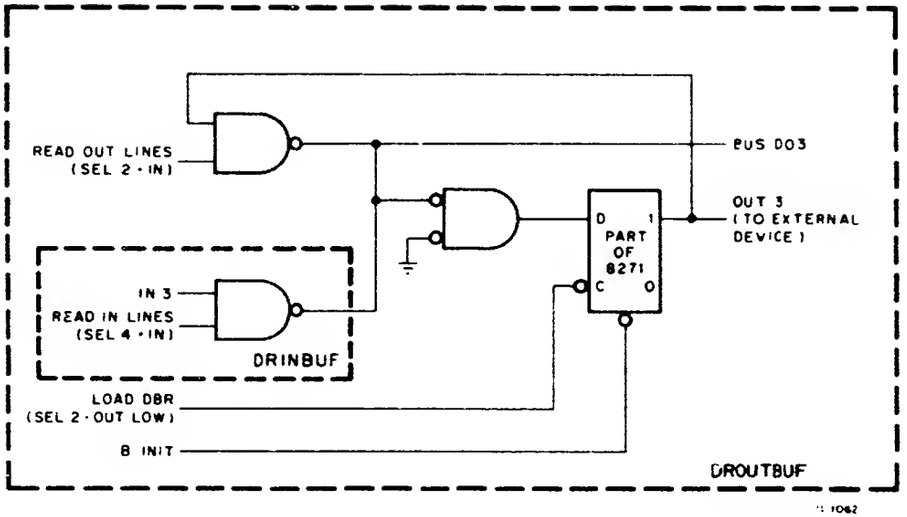


Figure 4-7 Input and Output Buffers, Simplified Diagram (one bit position)

When the register is to be loaded, the program places the appropriate data on bus data line BUS D03 which serves as the data input to the flip-flop. When addressed for loading, the LOAD DBR signal is true (SEL 2 and OUT LOW both true) and is applied as the clock input to the flip-flop, thereby setting it to the appropriate state. The flip-flop output is applied to the OUT 3 line which is connected to the user's device. Note that OUT LOW is shown in the figure because bit 03 is in the low-order byte portion of the register. The OUT HIGH signal may also be true during load operations so that the high-order byte portion of the register can also be loaded.

The LOAD DBR signal is gated to produce the pulsed signals (NEW DATA READY) which are applied to the external device to inform the user that the output buffer register has been loaded. In effect, the NEW DATA READY signals load the buffer on its leading edge; therefore, the user's logic should use the trailing edge of the pulse to sample the data lines. The output buffer can be loaded with a full 16-bit word (DATO) or with either a high-order or low-order 8-bit byte (DATOB). Selection of a DATO or DATOB is dependent on the incoming address and the address selection circuits described in Paragraph 4.2.

4.6 INPUT BUFFER REGISTER (DRINBUF)

The input buffer is a 16-bit read-only register that receives data from the user's device for transmission to the Unibus. The logic for the low-order byte is shown on drawing DR-3, and logic for the high-order byte is shown on drawing DR-2. A simplified version of the DRINBUF logic (one bit position) is shown in Figure 4-7 and described below.

The input buffer is not a flip-flop register but consists simply of gates that strobe data from the external device onto the bus. The external device places the appropriate data level on the input line (IN 3) and this level is gated to the associated bus data line (BUS D03) when the input buffer is addressed for reading. When addressed for reading, the READ IN LINES signal is true (SEL 4 and IN both true) and enables the gate. This READ IN LINES signal is gated to produce a pulsed signal (DATA TRANSMITTED) that is returned to the external device to inform the user that the input buffer has been read. The data lines should be held until the trailing edge of the DATA TRANSMITTED pulse. The entire word is read even if a byte instruction is used. Therefore, if an attempt is made to read only the low-order byte, for example, data on the high-order byte lines is also transferred to the bus.

G3

CHAPTER 5
MAINTENANCE

5.1 INTERFACE TESTING

Checkout and testing of the DR11-C is accomplished by using the MAINT cable supplied with the interface. Rather than using the two M971 connector modules to cable user signals to and from the external device, the maintenance cable plugs into the two connectors on the M7860 module and jumpers the DR11-C output lines to the input lines as shown in Figure 5-1.

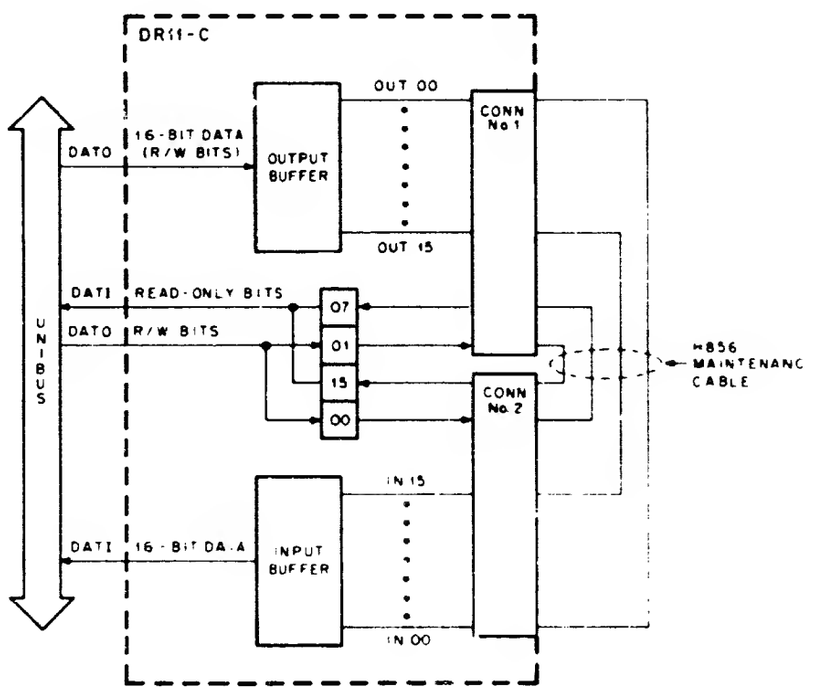


Figure 5-1 DR11-C Bits Jumpered by Maintenance Cable

As can be seen in the figure, any 16-bit word loaded from the bus into the output buffer is fed back into the input buffer for reading from the bus. In this case, if the word that is read is identical to the word that had been loaded, it indicates that the input buffer, output buffer, and associated circuits are all functioning properly.

The MAINT cable also checks the bits in the status register with the exception of the two INT ENB bits which are read/write bits cleared by INIT and capable of being completely checked by the program. Bits 00 and 01 (CSR0 and CSR1) are loaded from the bus and then read back from bit positions 07 and 05 (REQUEST A and REQUEST B), respectively, as well as being read back from bit positions 00 and 01. In effect, a value is loaded into a CSR bit and read back from a REQUEST bit to check the status register logic and associated circuits.

5.2 CHECKOUT PROCEDURE

The following is a typical method of checking DR11-C interface operation that can be performed from the processor's console.

Step	Procedure
1	Connect the MAINT cable between Connector No. 1 and Connector No. 2 on the M7860 module.
	NOTE **MAINT cable must have a 180 degree twist in order to match signals in connectors No. 1 and No. 2.**
2	Load DROUTBUF with a specific word (DATO operation).
3	Read DRINBUF (DATI operation). Verify that the word read is identical to the word loaded in Step 2 above.
4	Load DRCSR bits 00 and 01 (DATO operation).
5	Read DRCSR bits 07 and 15 (DATI operation). Verify that bit 07 is identical to the value loaded into bit 00 (Step 4) and that bit 15 is identical to bit 01.

CHAPTER 6
EXAMPLES

6.1 BASIC INTERFACE

Figure 6-1 illustrates a typical user's device interface, consisting of a basic control section and a data assembly register.

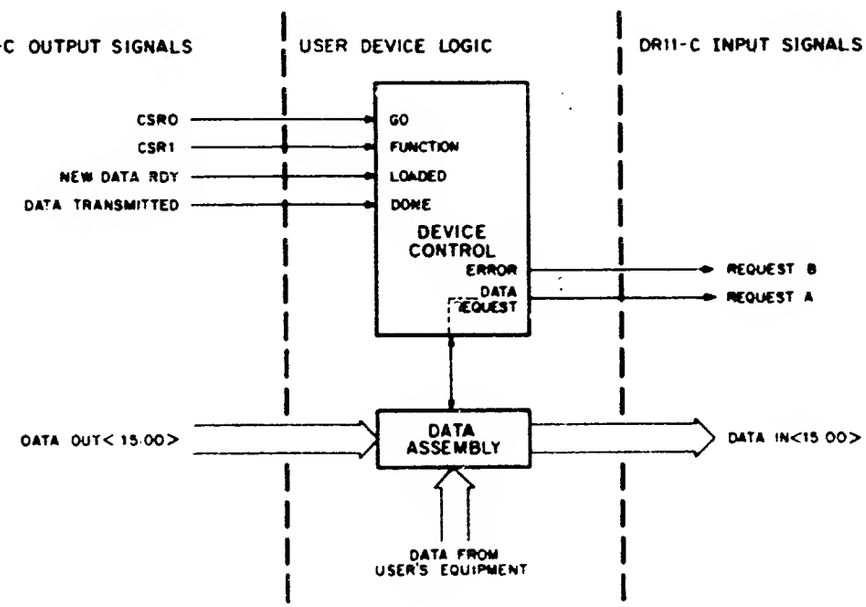


Figure 6-1 Basic Interface

Operation of the interface is initiated by the GO level. The FUNCTION bit informs the device whether it is to perform a read or write operation. When data is ready for transfer to the Unibus or data is required from the Unibus, a low-to-high transition on DATA REQUEST activates the REQUEST A line. The REQUEST A line initiates an interrupt sequence provided the INT ENB A bit in the DR11-C status register has been set. If the desired function is to load data into the user device, a LOADED (NEW DATA READY) pulse informs the device control when the data is ready for transfer. If a write function has been selected, a DONE (DATA TRANSMITTED) pulse informs the device control when the DR11-C has completed strobing of the data. The ERROR

L3

line becomes true if some type of error condition occurs in the device. This ERROR line (REQUEST B) can either be monitored by the program or can be used to initiate an interrupt sequence (provided INT ENB B is set) to cause the program to branch to an error handling routine.

With the signals available to the user, there are many possible variations to this basic interface. For example, the two CSR bits (CSR0 and CSR1) could provide a 2-bit code to select one of four operations to be performed by the external device.

Another possibility would be to use one REQUEST line for interrupts and the other REQUEST line for a flag (associated INT ENB not used) in order to inform the program of the desired operation to be performed on the data.

A third possibility might be to use the two CSR bits as a selection code and have DONE (NEW DATA READY) serve as a start command so that device operation begins as soon as the DR11-C output buffer has been loaded from the bus.

6.2 INTERRUPT SERVICED INTERFACE

Figure 6-2 is an example of an interrupt serviced interface that employs a DR11-C to interface an analog-to-digital converter (ADC) to the Unibus. This interface allows the processor to concurrently execute instructions of another program while the ADC performs a cycle of operation. The processor responds to a READY (CONVERSION COMPLETE) signal from the ADC by interacting with the device and analyzing the data after it has been collected. This interface eliminates the necessity of having the processor spend time testing for a ready signal.

Note that this example uses only the REQUEST A line. The available REQUEST B line can be used as an ERROR indicator, if desired, and the two CSR lines could be used to initiate other actions within the external device.

6.3 GENERATING REQUEST LINE LEVELS

Two request lines (REQUEST A, B) are furnished and may be asserted (+3V) by the user's device to initiate an interrupt sequence or to produce a flag that can be tested by the program. The request lines must be levels and must remain asserted for the entire interrupt sequence. Typically, they are generated in the user's device by a REQUEST flip-flop which is set by the device when an interrupt is requested and cleared by the interrupt service routine by means of the NEW DATA READY or DATA TRANSMITTED signals.

Figure 6-3 represents the control circuit necessary to generate the REQUEST A H and REQUEST B H signals. Similar logic could be used if it is desired to have CSR0 H and CSR1 H control the clearing of the REQUEST lines.

6.4 INTERPROCESSOR BUFFER

Two DR11-C interfaces can be interconnected to allow data transfers and intercommunication between two PDP-11 Systems. Figure 6-4 is a simplified diagram of this interconnection.

The two interconnecting cables are the same as the MAINT cable and may be procured in either 1-ft or 25-ft lengths. Maximum allowable cable length is 25 ft.

m3

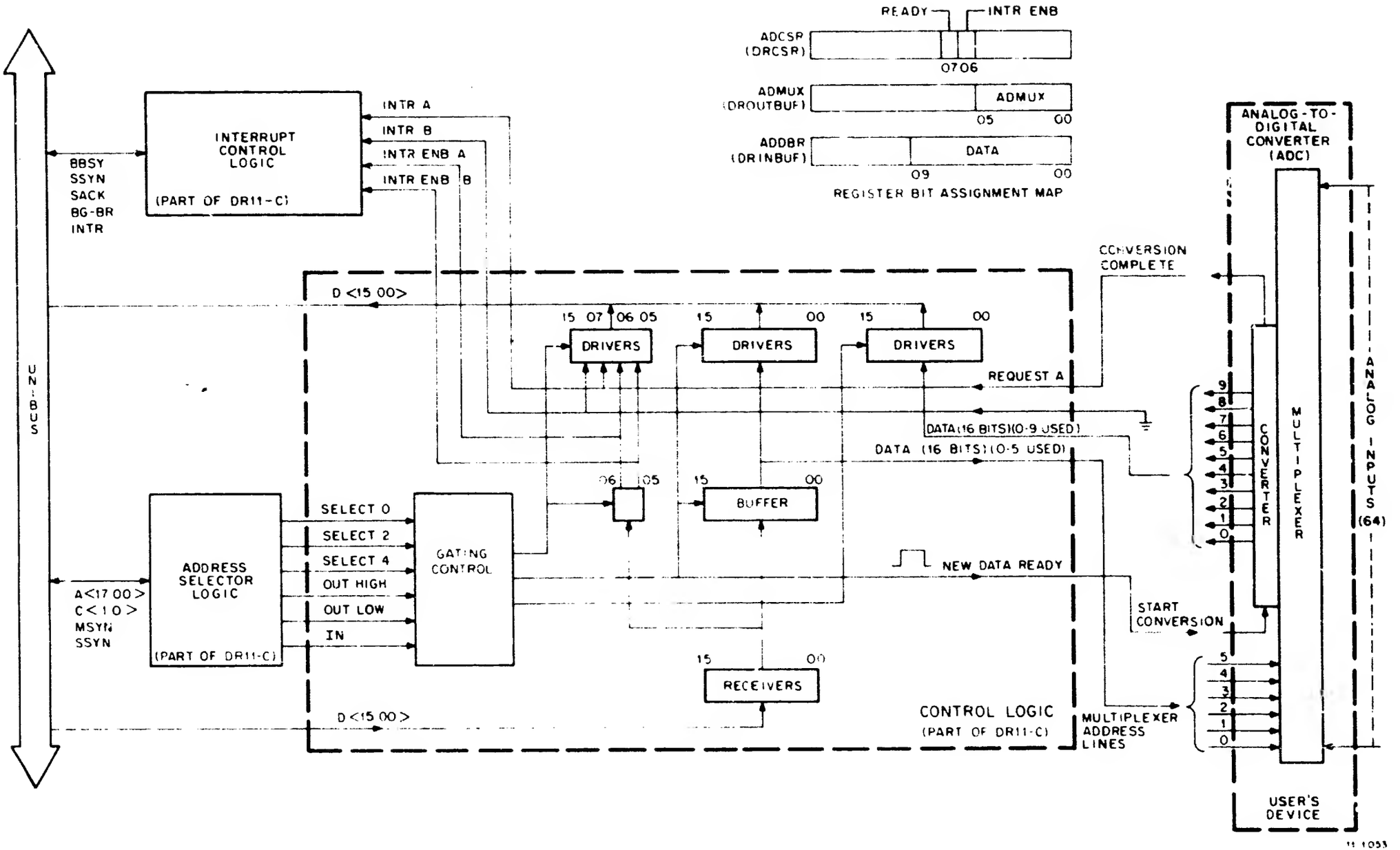


Figure 6-2 Interrupt Serviced Interface

A4

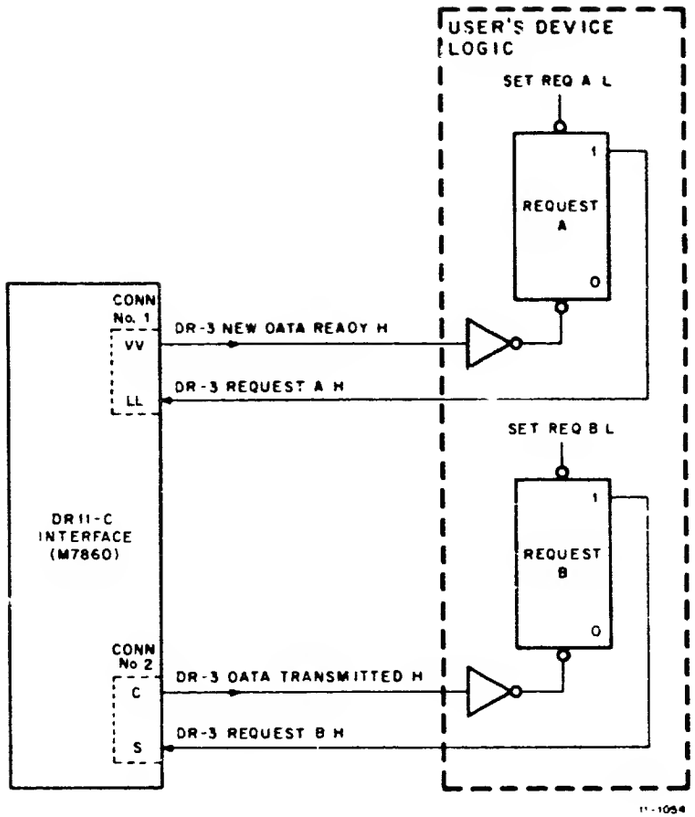


Figure 6-3 Request Line Control Logic

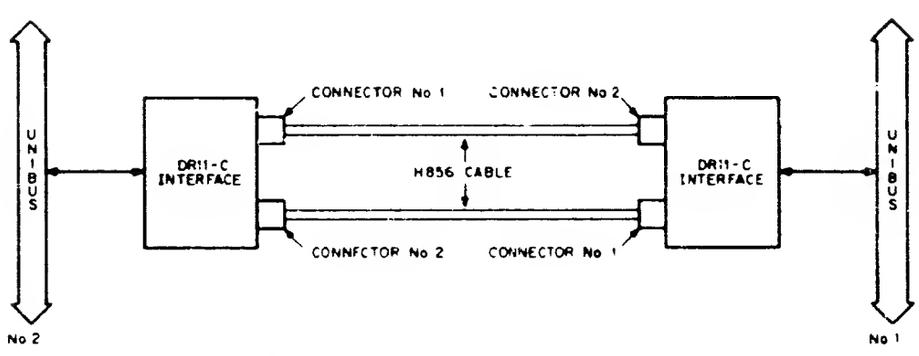


Figure 6-4 Interprocessor Buffer, Simplified Diagram

B4

The Connector No. 1 of the first DR11-C is connected to Connector No. 2 of the second DR11-C. This causes all of the output lines (OUT00 – OUT15) of the first interface to be connected to the corresponding input lines (IN00 – IN15) of the second interface (refer to pin connections given in Table 3-5). The CSR0 and CSR1 lines of the first unit are connected to the REQ A and B lines, respectively, of the second unit.

Connector No. 2 of the first unit is connected to Connector No. 1 of the second unit. This connects the IN lines and REQ lines of the first unit to the OUT lines and CSR lines of the second unit.

With the two PDP-11 buses interfaced in this manner, setting a CSR bit in one interface activates the REQ line in the other interface to initiate an interrupt sequence. Data can then be loaded from the bus into the DROUTBUF of the first unit for transfer to the DRINBUF of the second unit.

When DR11-Cs are used as interprocessor buffers, a power fail situation on either Unibus must be handled by the software. The software routine would be entered from the power fail trap vector and, by use of the REQUEST lines, would inform the other DR11-C that power is failing.

C4

CHAPTER 7
ENGINEERING DRAWING SET

A complete set of engineering drawings is provided with each DR11-C interface. These drawings are bound in a separate volume entitled, *DR11-C General Device Interface*, Engineering Drawings. The following paragraphs describe the signal nomenclature conventions used on the drawing set.

Signal names in the DR11-C print set are in the following basic form:

SOURCE	SIGNAL NAME	POLARITY

SOURCE indicates the drawing number of the print where the signal originates. The drawing number of a print is located in the lower right-hand corner of the print title block (DR-2, DR-3, or DR-4).

SIGNAL NAME is the proper name of the signal. The names used on the print set are also used in this manual for correlation between the two.

POLARITY is either H or L to indicate the voltage level of the signal: H means +3V; L means ground.

As an example, the signal:

DR-3 INT ENB A H

originates on sheet 3 of the M7860 module drawing and is read, "When INT ENB A is true, this signal is at +3V."

Unibus signal lines do not carry a SOURCE indicator. These signal names represent a bidirectional wire-ORed bus; as a result, multiple sources for a particular bus signal exist. Each Unibus signal name is prefixed with the word BUS.

Interface signals that are fed to the external device are preceded by the pin number in parentheses:

(1VV) NEW DATA READY H

Interface signals received from the external device are followed by the pin number in parentheses:

IN 6 (2PP)

In both of the above cases, the initial number in parentheses is the connector number (1 or 2), and the letter, or letters, are the pin number of that connector.

E4

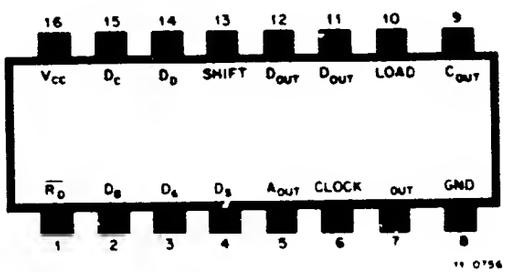
APPENDIX A
INTEGRATED CIRCUIT

There are five 8271 IC chips used in the DR11-C interface. Although this chip is designed as a 4-bit shift register, the shift input is disabled and each chip functions as four individual flip-flops. Four 8271 ICs are used for the 16-bit DROUTBUF register and the remaining IC is used for the four read/write bits in the DRCSR register.

Figure A-1 provides a circuit schematic, packaging diagram, and truth table for the 8271 IC.

Truth Table

Control State	Load	Shift
Hold	0	0
Parallel Entry	1	0
Shift Right	0	1
Shift Right	1	1



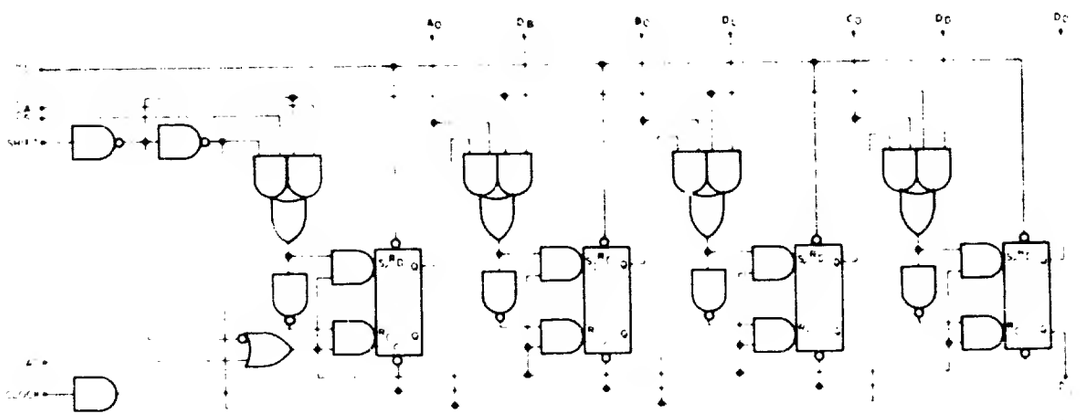


Figure A-1 8271 IC Circuit Schematic

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APPENDIX B
USE OF BB11

The BB11 Blank Mounting Panel is a prewired system unit designed for general interfacing. Figure B-1 illustrates the method of mounting a DR11-C interface into a BB11 system unit, assuming that the BB11 has slot 1 wired as a DD11-A or equivalent.

The first step is to mount the DR11-C in one of the four slots. Two of the remaining slots are used for the two M971 Cable Connector modules. This leaves 12 double-height slots available for mounting user interface logic.

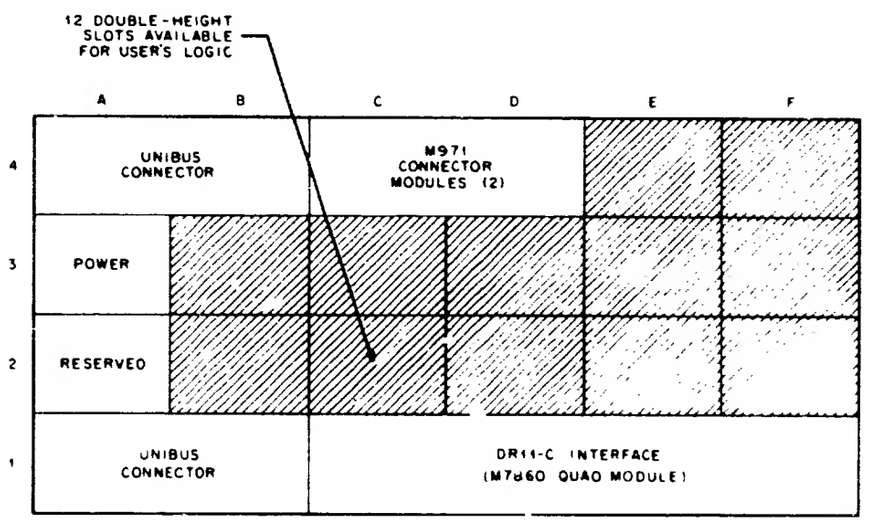

Figure B-1 DR11-C Mounted in BB11 System Unit